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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,180	PARK ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to the AMENDMENT filed 10/27/2005. Claims 1-20 are pending.

Claims 12-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse of Claims 1-11 and 16-20 in the reply filed on 7/28/2005.

Objection to the abstract in the prior Office Action is hereby withdrawn, in view of the Amendment.

Objection to the Claims in the prior Office Action is hereby withdrawn, in view of the Amendment.

Response to Arguments

Applicant's arguments filed 10/27/2005, with respect to the rejection of claims 1-11 and 16-20, under 35 U.S.C. 102(b) as being anticipated by Wrinn (U.S. Patent N0. 4,746,855), have been fully considered but they are not persuasive.

In response to Applicant's argument, in reference to independent claims 1, 8 and 16, The Examiner concedes that Wrinn fails to disclose "a pattern memory for storing the input signal patterns and the output signal patterns". However, under a new ground of rejection, Dehara (U.S. Patent No. 4,775,977) discloses "a pattern memory (1A) for storing a driver pattern and an expected pattern", where the driver and the expected pattern corresponds to the claimed input signal and the output signal patterns, respectively (see Abstract, line 2, and Figure 1).

Claims 1-11 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wrinn (U.S. Patent N0. 4,746,855) in view of Dehara (US Patent No. 4,775,977), as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wrinn (U.S. Patent N0. 4,746,855) in view of Dehara (U.S. Patent No. 4,775,977).

Regarding independent Claim 1, Wrinn substantially discloses a semiconductor device test system (Figure 1), comprising:

A plurality of comparator and driver units (twelve channel driver/detectors 16 for channels A to L) each comparator and driver unit (16) comprising a driver (26) configured to drive an input signal pattern from the test controller 22 by bus 24 to be applied to two or more input pins of semiconductor devices 40 on PCB under test 13 by providing inputs to test pins 44, and sensing the resulting conditions at the nodes common to leads to the device 40 being tested. In testing individual devices 40,

selected channels A-L are connected to selected test pins 44 by activating the appropriate relays 36 by relay controller 20, operating under relay control signals provided by controller 22 over bus 24. Test controller 22 also provides test control signals over bus 24 to operate channel drivers 26 to provide test signal inputs and detectors 28 to detect the test outputs while switch 29 is closed and switch 30 is open. The test outputs are provided to test controller 22, and compared with expected test outputs, (see, Figures 1, 2, 3 and 5, and operation Col. 4, lines 14-35).

It is noted with respect to claimed limitation of "a driver configured to drive an input signal pattern to be applied to two or more input pins of the semiconductor device", according to Wrinn, driver (26) of channels (A to L) drives a group of pin nodes 12 connected to semiconductor device 40 from the channel nodes 14, via relays 36 in multiplexer 10 controlled by relay controller 20, Figures 1, 2, 3 and 5, as described: " In group 32 or group 34, of relay multiplexer 10, it is possible to make a connection between any pin node or any channel node of the group with any other pin node or channel node of the group, through multiple or single closed relays. The combinations of channel nodes 14 are assigned to pin nodes 12 in a fully combinatorial manner; i.e., every possible unique combination of two of the twelve channels A to L. Each channel (A-L) is connectable to eleven test pin nodes (Figures 3, 5 and col. 2, lines 55-60). For example, channel A is connected to pins 1, 2, 4, 7, 11, 16, 22, 29, 37, 46 and 56 of group 32 through relays 36. Similarly, other connection combination of eleven pins applies to the rest of the channels (B-L). Therefore, each driver (26) of channels (A to

L) is capable of applying test signals to a group of pin nodes 12 (eleven test pin nodes), thus meeting the claimed requirements.

A plurality of control units (each comprising a group of eleven relays 36 corresponding to each channel) of the relay multiplexer 10 in group 32, and each configured to electrically connect a corresponding comparator and driver unit (16) to test pins 44 through pin nodes 12 of the semiconductor device 40 in response to a control signal from relay controller 20. The pins 44 of the semiconductor device 40 are divided into pin groups corresponding to channels (A-L), each pin group (channel) having K=11 number of pins (eleven test pin nodes per channel in group 32, Figure 5), where K=11 is an integer greater than 1.

Wrinn fails to disclose "a pattern memory for storing the input signal patterns and the output signal patterns". However, in analogous art, Dehara discloses "a pattern memory (1A) for storing a driver pattern and an expected pattern", where the driver and the expected pattern corresponds to the claimed input signal and the output signal patterns, respectively (see Abstract, line 2, and Figure 1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a pattern memory in the tester of Wrinn, as taught by Dehara, for the purpose of generating a driver pattern applied to a DUT and an expected pattern to be utilized as a reference pattern for comparison with the output pattern produced by the DUT in response to the input driver pattern, wherein decision of the DUT as to the performance thereof is made on the result of the comparison.

Regarding Claims 2, 3, Wrinn discloses control unit comprising a group of eleven relays 36 corresponding to each channel of the relay multiplexer 10 in group 32, having K number of inputs, where K=11, wherein each control unit is configured to receive the control signal via a data bus 19 from relay controller 20.

Regarding Claim 4, Wrinn discloses wherein the test pins 44 of each pin group of the semiconductor device 40 corresponding to output pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns to provide test signal inputs to device 40 and an output pattern memory for storing output signal patterns (expected test outputs) and wherein the output pattern memory stores output signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding Claim 5, Wrinn discloses wherein the test pins 44 of each pin group of the semiconductor device 40 corresponding to input pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted output signal patterns (expected test outputs) and wherein the input pattern memory stores input signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes.

With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding Claim 6, Wrinn discloses wherein the test pins 44 of each pin group of the semiconductor device 40 corresponding to input and/or output pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted output signal patterns (expected test outputs) and wherein the input pattern memory stores input signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding Claim 7, Wrinn discloses wherein the test pins 44 of each pin group of the semiconductor device 40 corresponding to output pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns to provide test signal inputs to device 40 and an output pattern memory for storing output signal patterns (expected test outputs), and where the (expected test outputs) are stored in an (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at

the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding independent Claim 8, Wrinn substantially discloses a method of testing a semiconductor device using the semiconductor device test system (Figures 1, 2, 3 and 5), comprising:

Selecting pins (test pins 44) from among a plurality of pins of the semiconductor device 40 on PCB under test 13.

Dividing the selected pins (test pins 44) into a plurality of pin groups corresponding to each channel (A-L), disclosed as follows: Each channel (A-L) is connectable to eleven test pin nodes (Figures 3, 5 and col. 2, lines 55-60). For example, channel A is connected to pins 1, 2, 4, 7, 11, 16, 22, 29, 37, 46 and 56 of group 32 through relays 36. Similarly, other connection combination of eleven pins applies to the rest of the channels (B-L). The test pins 44 of the semiconductor device 40 are divided into pin groups corresponding to channels (A-L), each pin group (channel) having K=11 number of pins (eleven test pin nodes per channel in group 32, Figure 5), where K=11 is an integer greater than 1.

Generating a control signal from relay controller 20.

Electrically connecting a comparator and driver unit (16) to switch 29 connected to channel line 18 and in turn to a single pin 44 of the semiconductor device, which is

connectable from a pin node 12 through a relay 36. "In group 32 or group 34, in typical operation, however, at any given time, each channel node would be connected to no more than one pin node, and each pin node would be connected to no more than one channel node".

The test controller 22 also provides test control signals over bus 24 to operate channel drivers 26 to provide test signal inputs and detectors 28 to detect the test outputs while switch 29 is closed and switch 30 is open. The test outputs are provided to test controller 22, and compared with expected test outputs, (see, Figures 1, 2, 3 and 5, and operation Col. 4, lines 14-35).

Wrinn fails to disclose "applying input signal patterns from an input pattern memory to input pins of the semiconductor device, and comparing data output from output pins of the semiconductor device with output signal patterns output from an output pattern memory". However, in analogous art, Dehara discloses "a pattern memory (1A) for storing a driver pattern and an expected pattern", where the driver and the expected pattern corresponds to the claimed input signal and the output signal patterns, respectively (see Abstract, line 2, and Figure 1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a pattern memory in the tester of Wrinn, as taught by Dehara, for the purpose of generating a driver pattern applied to a DUT and an expected pattern to be utilized as a reference pattern for comparison with the output pattern produced by the DUT in response to the input driver pattern, wherein decision of the DUT as to the performance thereof is made on the result of the comparison.

Regarding Claim 9, Wrinn discloses wherein the selected test pins 44 of each pin group of the semiconductor device 40 corresponding to input pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted output signal patterns (expected test outputs) and wherein the input pattern memory stores input signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding Claim 10, Wrinn discloses wherein the selected test pins 44 of each pin group of the semiconductor device 40 corresponding to output pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns to provide test signal inputs to device 40 and an output pattern memory for storing output signal patterns (expected test outputs) and wherein the output pattern memory stores output signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing

(using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding Claim 11, Wrinn discloses wherein all the test pins 44 of each pin group of the semiconductor device 40 corresponding to input and/or output pins, wherein the test controller 22 comprises memory including an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted output signal patterns (expected test outputs) and wherein the input pattern memory stores input signal patterns from an external device (external tester) coupled to the test controller 22 to provide test signals to nodes of the board under test and analyzing the resulting conditions at the nodes. With respect to claimed input and output pattern memory, Wrinn describes, "using a tester to provide test signals to nodes (using input pattern memory) of the board under test and analyzing (using output pattern memory) the resulting conditions at the nodes", (col. 1, lines 13-15).

Regarding independent Claim 16, Wrinn substantially discloses a method of testing a semiconductor device using the semiconductor device test system (Figures 1, 2, 3 and 5), comprising:

Selectively (through relay 36) connecting a pin (12) from comparator and driver unit (16) to switch 29 connected to channel line 18 of the test system to a pin 44 of the semiconductor device 40 based on a control signal from the relay controller 20. "As is seen in Figure 4, each relay 36 makes a channel node 14 connectable to a pin node 12

by a normally open switch 38 controlled by TTL signals from controller 20 (via means not shown).

Wrinn fails to disclose "applying input signal patterns from an input pattern memory to input pins of the semiconductor device, and comparing data output from output pins of the semiconductor device with output signal patterns output from an output pattern memory". However, in analogous art, Dehara discloses "a pattern memory (1A) for storing a driver pattern and an expected pattern", where the driver and the expected pattern corresponds to the claimed input signal and the output signal patterns, respectively (see Abstract, line 2, and Figure 1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a pattern memory in the tester of Wrinn, as taught by Dehara, for the purpose of generating a driver pattern applied to a DUT and an expected pattern to be utilized as a reference pattern for comparison with the output pattern produced by the DUT in response to the input driver pattern, wherein decision of the DUT as to the performance thereof is made on the result of the comparison.

Regarding Claim 17, Wrinn discloses wherein the pin of the test system comprises a comparator and driver unit 16, comprising a comparator (detectors 28) configured to compare an output pattern from an output pin 44 of the semiconductor device 40 with a predetermined output pattern and a driver 26 configured to drive an input pattern for an input pin 44 of the semiconductor device 40, and wherein the comparator and driver unit is selectively connected (trough a relay 36) to the pin 44 of

the semiconductor device 40 based on the control signal from controller 20. Test controller 22 also provides test control signals over bus 24 to operate channel drivers 26 to provide test signal inputs and detectors 28 to detect the test outputs while switch 29 is closed and switch 30 is open. The test outputs are provided to test controller 22, and compared with expected test outputs, (see, Figures 1, 2, 3 and 5, and operation Col. 4, lines 14-35).

Regarding Claim 18, Wrinn discloses wherein the pins 44 of the semiconductor device 40 are divided into pin groups corresponding to channels (A-L), each pin group (channel) having K=11 number of pins (eleven test pin nodes per channel in group 32, Figure 5), where K=11 is an integer greater than 1.

Regarding Claim 19, Wrinn discloses wherein the pin (12) of the test system is selectively connected (through relay 36) from comparator and driver unit (16) to switch 29 connected to channel line 18 to a pin 44 of the semiconductor device 40 based on a control signal from the relay controller 20. "As is seen in Figure 4, each relay 36 makes a channel node 14 connectable to a pin node 12 by a normally open switch 38 controlled by TTL signals from controller 20 (via means not shown).

Regarding Claim 20, Wrinn discloses wherein the pin of the test system comprises a comparator and driver unit 16 and a control unit (each comprising a group of eleven relays 36 corresponding to each channel) of the relay multiplexer 10 in group 32, wherein the control unit is configured to electrically connect a corresponding comparator and driver unit (16) to test pins 44 through pin nodes 12 of the semiconductor device 40 in response to a control signal from relay controller 20.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arai (U.S. Patent No. 5,701,306) discloses, Figure 7, a high speed LSI tester 70, which includes a test pattern memory 77 and an expected value pattern memory 78, which are coupled as shown. The test pattern memory 77 stores a number of test patterns to be supplied to the terminals of the LSI 700, which are sequentially supplied from the high speed LSI tester 70 through the output drivers 71 to 73 to the LSI 700. The comparator 75 compares the received looped-back data with the expected value pattern stored in the expected value pattern memory 78.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: _____.

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